

IN THE  
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Kenneth P. Parker

Serial No.: Unknown

Examiner: Unknown

Filing Date: Unknown

Group Art Unit: Unk

Title: METHODS AND APPARATUS FOR MINIMIZING CURRENT SURGES DURING INTEGRATED  
CIRCUIT TESTING

COMMISSIONER FOR PATENTS  
Washington, D.C. 20231

5/IDS  
E. Willis  
10-30-01

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- ☒ under 37 CFR 1.97(b), or  
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)
- ☐ under 37 CFR 1.97(c) together with either a:  
☐ Statement under 37 CFR 1.97(e), or  
☐ a \$180.00 fee under 37 CFR 1.17(p), or  
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)
- ☐ under 37 CFR 1.97 (d) together with a:  
☐ Statement under 37 CFR 1.97(e), and  
☐ a petition under 37 CFR 1.97(d)(2), and  
☐ a \$130.00 petition fee set forth in 37 CFR 1.17(i).  
(Filed after final action or notice of allowance, whichever occurs first, but before payment of the issue fee)

Please charge to Deposit Account **50-1078** the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-1078** pursuant to 37 CFR 1.25.

☒ Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Citation together with copies, of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. **EL657274564US**

Date of Deposit July 19, 2001

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Washington, D.C. 20231.

By

Typed Name: Gregory W. Osterloth

Respectfully submitted,

Kenneth P. Parker

By

Gregory W. Osterloth, Esq.

Attorney/Agent for Applicant(s)  
Reg. No. 36,232

Date: July 19, 2001



FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR  
APPLICANT'S INFORMATION DISCLOSURE  
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.

10001121-1

SERIAL NO.

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APPLICANT

Kenneth P. Parker

FILING DATE

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jc971 U.S. PTO  
09/908948

07/19/01

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

| EXAMINER<br>INITIAL |    | DOCUMENT<br>NUMBER | DATE | NAME | CLASS | SUB<br>CLASS |
|---------------------|----|--------------------|------|------|-------|--------------|
|                     | 1A |                    |      |      |       |              |
|                     | 1B |                    |      |      |       |              |
|                     | 1C |                    |      |      |       |              |
|                     | 1D |                    |      |      |       |              |
|                     | 1E |                    |      |      |       |              |
|                     | 1F |                    |      |      |       |              |
|                     | 1G |                    |      |      |       |              |
|                     | 1H |                    |      |      |       |              |
|                     | 1I |                    |      |      |       |              |
|                     | 1J |                    |      |      |       |              |
|                     | 1K |                    |      |      |       |              |

## FOREIGN PATENT DOCUMENTS

|  |    | DOCUMENT<br>NUMBER | DATE | NAME | CLASS | SUB<br>CLASS | TRANSLATION |    |
|--|----|--------------------|------|------|-------|--------------|-------------|----|
|  |    |                    |      |      |       |              | YES         | NO |
|  | 1L |                    |      |      |       |              |             |    |
|  | 1M |                    |      |      |       |              |             |    |
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|  | 1O |                    |      |      |       |              |             |    |
|  | 1P |                    |      |      |       |              |             |    |

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

|    |  |
|----|--|
| 1Q | "A Logic Design Structure for LSI Testability", E.B. Eichelberger and T.W. Williams, Proc. 14th Design Automation Conf. IEEE Pub. 77CH1216-1C, June 1977, pp 462-468                           |
| 1R | "The Challenges of Design and Test for the World Wide Web", P. Gelsinger, Proc. International Test Conference, IEEE Pub. 99CH37034, Sept 1999, p 12  |
| 1S | "Enhancing Testability of Large; Scale Integrated Circuits Via Test Points and Additional Logic", M.J.Y. Williams and J.B Angell, IEEE Trans. on Computers, Jan 1973, vol C-22, no.1, pp 46-60 |

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DATE CONSIDERED

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|  | 2O |                    |      |      |       |              |             |    |
|  | 2P |                    |      |      |       |              |             |    |

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

|    |  |
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| 2Q | "Design for Testability - A Survey", T.W. Williams and K.P. Parker, Proceedings of the IEEE, Jan. 1983, Vol 71, no. 1, pp 98-112 |
| 2R | "The Boundary Scan Cell", Texas Instruments, JTAG IEEE 1149.1/P1149.4 Tutorial, Sept. 1997, Tut.I-20, Tut II-24-26               |
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